REMARKS

Claims 1-20 are in this application and are presented for consideration. By this Amendment, Applicant has amended claims 1, 12 and 17.

The present invention relates to a process for producing a contact structure for connecting two substrates. The process comprises the step of applying solder material to terminal areas of a first substrate to form electrically conductive spacing metallizations with the solder material. The spacing metallizations are in direct contact with the terminal areas of the first substrate. The process further comprises the step of bonding the first substrate with a second substrate. The bonding between the terminal areas of the first substrate and a contact surface area of the second substrate is performed by means of a partial fusion of the spacing metallizations during the bonding action. The partial fusion of the spacing metallizations leaves an essential part of the spacing metallizations in its solidified state for providing between the terminal areas and the contact surface area. The process advantageously allows good electrical connection, a good mechanical connection and provides for is the necessary spacing with a simple and effective procedure. The prior art as a whole fails to disclose such features or advantages.

The present application names joint inventors. The Office Action states that in considering patentability of the claims under 35 U.S.C. 103(a), the Examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. To the best of Applicant's knowledge, the subject matter of the various claims were commonly owned at the time the invention was

made.

Claims 1-4, 12-15 and 17-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Myers et al. (US 5,400,950) in view of Gotman (US 4,404,453).

Myers et al. relates to a method for controlling solder bump height for flip chip integrated circuit devices. A flip chip 12 is mounted to a circuit board, which is represented by a substrate 10. A number of bead-like projections are formed on one surface of the flip chip 12 to serve as terminals. These projections electrically interconnect the flip chip 12 to a conductor pattern formed on the substrate 10. The solder bumps 16 are positioned on the flip chip 12 such that, when registered with a conductor pattern on the substrate 10, each of the solder bumps 16 are mated with a corresponding conductor 14. The height of the solder bumps 16 is determined by the effect of a number electrically inactive, dummy solder bumps 20. The solder bumps 20 are positioned on a pad 22 formed on the substrate 10. The solder bumps 16 are deposited on a surface of the flip chip 12 to bond the flip chip 12 to the substrate 10. The flip chip 12 is then soldered to the substrate 10 using a reflow technique which heats the solder bumps 16 and dummy bumps 20 to a temperature above the melting point of the solder alloy.

Myers et al. fails to teach or suggest the combination of an electrically conductive spacing between the terminal areas of the first substrate and a contact surface area of a second substrate. This electrically conductive spacer is significant in the present invention because it provides for a good electrical connection while achieving a spacing function between the first substrate and the second substrate. Myers et al. fails to teach or suggest that the dummy bumps 20 serve as an electrical connection. In fact, Myers et al. merely suggests that the dummy

bumps 20 provide for only a spacing function. Myers et al. clearly discloses that the dummy bumps 20 are electrically inactive. (Column 5, lines 35-36). As such, Myers et al. only suggests that the dummy bumps 20 serve as spacers and disadvantageously fail to provide any electrical conductivity. In the present invention, the spacing metallizations advantageously provide both a mechanical and an electrical function. The dummy bumps 20 disclosed in Myers et al. fail to provide such a duel function. As such, the prior art as a whole takes a different approach and fails to teach or suggest the features or advantages of the present invention.

Gotman fails to provide any teaching or suggestion which would lead the person of ordinary skill in the art toward the combination claimed. Gotman discloses bonding a chip 20 and substrate 10 by backwards heating the chip 20 to melt solder globules 22 and 12 arranged on contact pairs 21 and 11. However, the references together provide no basis which would lead or direct the person of ordinary skill in the art toward the combination as claimed. Gotman fails to disclose the electrical and physical connection and spacing of the present invention. Due to the complete reflow or melting of the globules 12 and 22 in Gotman, there cannot be any spacing action accomplished by the globules 22 and 12. In contrast to the present invention, Gotman teaches that the spacing function is achieved by contact pairs 21 and 11. In the present invention, an essential part of the spacing metallizations are left in its solidified state to provide spacing as well as an electrical connection between the terminal areas and the contact surface area. The references together provide no direction to providing such the combination claimed. The references provide no direction or using teachings of Gotman to modify Myers et al. There is no teaching and no suggestion in the references as a whole to provide electrically conductive

spacing metallizations. As such, the prior art as a whole teaches a different approach and fails to provide any motivation for the features or advantages of the present invention. Accordingly, Applicant respectfully requests that the Examiner favorably consider claims 1, 12 and 17 and all claims that respectively depend thereon.

Claims 5-9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Myers et al. in view of Leicht et al. (US 5,551,627). Although Leicht et al. teaches a solder connection structure that uses different types of materials that have different melting temperatures, the references as a whole fail to suggest the combination of features claimed. Specifically, Myers et al. fails to teach or suggest the combination of electrically conductive spacing metallizations between the terminal areas of the first substrate and the contact surface area of the second substrate. The references do not suggest the invention and therefore all claims define over the prior art as a whole.

The prior art as a whole fails to direct the person of ordinary skill in the art toward the feature of the invention. Further, the invention includes cooperating features which provide particular advantages which are neither taught nor suggested by the prior art. Accordingly, Applicant requests that the Examiner favorably consider the amended claims in light of the discussion above.

Further and favorable consideration on the merits is requested.

Respectfully submitted
for Applicant,

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Attached: Petition for One Month Extension of Time

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SHOULD ANY OTHER FEE BE REQUIRED, THE PATENT AND TRADEMARK OFFICE IS HEREBY REQUESTED TO CHARGE SUCH FEE TO OUR DEPOSIT ACCOUNT 13-0410.